CLAIMS

1. A circuit for computing a product of a constant and a mixed number power of two, said mixed number comprising an integer portion and a fraction portion, said circuit comprising:

a first register for storing the constant;

a second register for storing the integer portion and the fraction portion;

a memory for storing a plurality of values, each of said plurality of values corresponding to a particular one of a corresponding plurality of fractions, wherein each one of said plurality of values is two to the exponential fraction corresponding to the one of said plurality of values;

a third register for storing a particular one of the plurality of values, said particular one of the plurality of values corresponding to the fraction portion;

a multiplier circuit for multiplying the contents of the third register by the contents of the first register, thereby resulting in a product; and

the product being shifted a certain number of times, the certain number of times equal to the integer portion.

2. The circuit of claim 1, wherein the second register comprises:

a first one or more bits for storing the integer portion; and

a second one or more bits for storing the fraction portion.

3. The circuit of claim 2, further comprising:

a shift register for storing the product and shifting the product the certain number of times.

4. The circuit of claim 3, wherein the first one or more bits are decremented after each shift of the shift register.

5. The circuit of claim 4, wherein the shift register shifts until the first one or more bits are decremented to zero.

6. The circuit of claim 1, wherein the plurality of values comprises at least four values.

7. A method for computing a product of a constant and a mixed number power of two, said mixed number comprising an integer portion and a fraction portion, said method comprising:

receiving the constant;

receiving the integer portion

receiving the fraction portion;

providing the fraction portion to a memory storing a plurality of values, each of said plurality of values corresponding to a particular one of a corresponding plurality of fractions, each one of said plurality of values being two to the exponential fraction corresponding to the one of said plurality of values;

receiving a particular one of the plurality of values, said particular one of the plurality of values corresponding to the fraction portion;

multiplying the constant by the particular one of the plurality of values, thereby resulting in a product; and

shifting the product a certain number of times, the certain number of times equal to the integer portion.

8. The method of claim 7, further comprising:

decrementing the constant after shifting the product.

9. The method of claim 8, further comprising shifting until the constant is decremented to zero.

10. The method of claim 7, wherein the plurality of values comprises at least four values.

11. A video decoder for decoding compressed video data, said video decoder comprising:

a Huffman decoder for decoding quantized coefficients;

ainverse quantizern inverse quantizer for inverse quantizing the quantized coefficientsinverse quantizer, thereby resulting in inverse quantized coefficients; and

a rescaler for scaling the inverse quantized coefficients, said rescaler further comprising:

a first register for storing a constant;

a second register for storing an integer portion and a fraction portion;

a memory for storing a plurality of values, each of said plurality of values corresponding to a particular one of a corresponding plurality of fractions, each one of said plurality of values being two to the exponential fraction corresponding to the one of said plurality of values;

a third register for storing a particular one of the plurality of values, said particular one of the plurality of values corresponding to the fraction portion;

a multiplier circuit for multiplying the contents of the third register by the contents of the first register, thereby resulting in a product; and

the product being shifted a certain number of times, the certain number of times equal to the integer portion.

12. The video decoder of claim 11, wherein the second register comprises:

a first one or more bits for storing the integer portion; and

a second one or more bits for storing the fraction portion.

13. The video decoder of claim 12, wherein the inverse quantizer further comprises:

a shift register for storing the product and shifting the product the certain number of times.

14. The video decoder of claim 13, wherein the first one or more bits are decremented after each shift of the shift register.

15. The video decoder of claim 14, wherein the shift register shifts until the first one or more bits are decremented to zero.

16. The video decoder of claim 11, wherein the plurality of values comprises at least four values.